

WHAT IS CLAIMED IS:

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1. A data processor comprising:

an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline;

a data cache capable of storing data values used by said pending instruction;

a plurality of registers capable of receiving said data values from said data cache;

a load store unit capable of transferring a first one of said data values from said data cache to a target one of said plurality of registers during execution of a load operation;

a shifter circuit associated with said load store unit capable of one of a) shifting, b) sign extending, and c) zero extending said first data value prior to loading said first data value into said target register; and

bypass circuitry associated with said load store unit capable of transferring said first data value from said data cache directly to said target register without processing said first data value in said shifter circuit.

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1 2. The data processor as set forth in Claim 1 wherein said
2 bypass circuitry transfers said first data value from said data
3 cache directly to said target register during a load word
4 operation.

1 3. The data processor as set forth in Claim 2 wherein said
2 bypass circuitry transfers said first data value from said data
3 cache directly to said target register at the end of two machine
4 cycles.

1 4. The data processor as set forth in Claim 1 wherein said
2 shifter circuit one of a) shifts, b) sign extends, and c) zero
3 extends said first data value prior to loading said first data
4 value into said target register during a load half-word operation.

1 5. The data processor as set forth in Claim 4 wherein said
2 shifter circuit loads said shifted first data value into said
3 target register at the end of three machine cycles.

1 A1 6. The data processor as set forth in Claim 1 wherein said
2 shifter circuit one of a) shifts, b) sign extends, and c) zero
3 extends said first data value prior to loading said first data
4 value into said target register during a load byte operation.

1 7. The data processor as set forth in Claim 6 wherein said
2 shifter circuit loads said shifted first data value into said
3 target register at the end of three machine cycles.

1 8. The data processor as set forth in Claim 1 wherein said
2 bypass circuitry comprises a multiplexer having a first input
3 channel coupled to a data output of said data cache.

1 9. The data processor as set forth in Claim 8 wherein said
2 multiplexer has a second input channel coupled to an output of said
3 shifter circuit.

1 A) 10. For use in a processor comprising an N-stage execution
2 pipeline, a data cache, and a plurality of registers, a method of
3 loading a first data value from the data cache into a target one of
4 the registers, the method comprising the steps of:

5 determining if a pending instruction in the execution
6 pipeline is one of a load word operation, a load half-word
7 operation, and a load byte operation;

8 in response to a determination that the pending
9 instruction is a load half-word operation, transferring the first
10 data value from the data cache to a shifter circuit and shifting
11 the first data value prior to loading the first data value into the
12 target register; and

13 in response to a determination that the pending
14 instruction is a load byte operation, transferring the first data
15 value from the data cache to a shifter circuit and shifting the
16 first data value prior to loading the first data value into the
17 target register

18 in response to a determination that the pending
19 instruction is a load word operation, transferring the first data
20 value from the data cache directly to the target register without
21 processing the first data value in the shifter circuit.

1 **A1** 11. The method as set forth in Claim 10 wherein the step of
2 transferring the first data value requires two machine cycles
3 during a load word operation.

1 12. The method as set forth in Claim 10 wherein the step of
2 transferring the first data value requires three machine cycles
3 during a load half-word operation.

1 13. The method as set forth in Claim 10 wherein the step of
2 transferring the first data value requires three machine cycles
3 during a load byte operation.

1 A) 14. A processing system comprising:
2 a data processor;
3 a memory coupled to said data processor;
4 a plurality of memory-mapped peripheral circuits coupled
5 to said data processor for performing selected functions in
6 association with said data processor, wherein said data processor
7 comprises:

8 an instruction execution pipeline comprising N
9 processing stages, each of said N processing stages capable of
10 performing one of a plurality of execution steps associated
11 with a pending instruction being executed by said instruction
12 execution pipeline;

13 a data cache capable of storing data values used by
14 said pending instruction;

15 a plurality of registers capable of receiving said
16 data values from said data cache;

17 a load store unit capable of transferring a first
18 one of said data values from said data cache to a target one
19 of said plurality of registers during execution of a load
20 operation;

21 a shifter circuit associated with said load store
22 unit capable of one of a) shifting, b) sign extending, and c)

23 A1 zero extending said first data value prior to loading said
24 first data value into said target register; and
25 bypass circuitry associated with said load store
26 unit capable of transferring said first data value from said
27 data cache directly to said target register without processing
28 said first data value in said shifter circuit.

1 15. The processing system as set forth in Claim 14 wherein
2 said bypass circuitry transfers said first data value from said
3 data cache directly to said target register during a load word
4 operation.

1 16. The processing system as set forth in Claim 15 wherein
2 said bypass circuitry transfers said first data value from said
3 data cache directly to said target register at the end of two
4 machine cycles.

1 17. The processing system as set forth in Claim 14 wherein
2 said shifter circuit one of a) shifts, b) sign extends, and c) zero
3 extends said first data value prior to loading said first data
4 value into said target register during a load half-word operation.

1 A1 18. The processing system as set forth in Claim 17 wherein
2 said shifter circuit loads said shifted first data value into said
3 target register at the end of three machine cycles.

1 19. The processing system as set forth in Claim 14 wherein
2 said shifter circuit one of a) shifts, b) sign extends, and c) zero
3 extends said first data value prior to loading said first data
4 value into said target register during a load byte operation.

1 20. The processing system as set forth in Claim 19 wherein
2 said shifter circuit loads said shifted first data value into said
3 target register at the end of three machine cycles.

1 21. The processing system as set forth in Claim 14 wherein
2 said bypass circuitry comprises a multiplexer having a first input
3 channel coupled to a data output of said data cache.

1 22. The processing system as set forth in Claim 21 wherein
2 said multiplexer has a second input channel coupled to an output of
3 said shifter circuit.